

3x-channel video analyzer for 3D image reconstruction

Completed project - December 2006

The analyzer is intended for image analysis and processing. Three CMOS sensors are supplying data for subsequent 3D image reconstruction, according to a user-defined algorithm.

AVNET (Silica) debugging boards and Texas Instruments 6416 DSK are applied for the controller. User-defined video input daughterboard has been developed for sensor`s connectivity. Micron MT9-SOC CMOS video-sensor with reading speed of 25 frames per second is used.

Application-specific image processing filters and embedded DSP/BIOS software are developed. User applications and drivers for the embedded Linux operating system are implemented. High-speed interfaces USB 2.0 and 2xEthernet 10/100 are used for connectivity link with a host workstation.



Specifications

FPGA-type	Xilinx Virtex4-FX12
DSP-type	Texas Instruments TMS320C6416T
Employed buses and FPGA memory interface	PLB, OPB, APU, OCM DDR SDRAM, BRAM, Flash
Employed buses and DSP memory interface	<ul style="list-style-type: none"> • EMIF • EDMA • GPIO • SDRAM • EEPROM
Employed connectivity interfaces	<ul style="list-style-type: none"> • Tri-MAC Ethernet 10/100 • USB 2.0 • UART
Developed IP cores	<ul style="list-style-type: none"> • Application-specific image processing filters • FPGA to DSP bridge
Peculiarities	<ul style="list-style-type: none"> • Sensor`s system frequency 27 MHz • Processor: PowerPC 405-350 MHz • Operating system: MontaVista Linux, DSP\BIOS
Design tools	ISE Xilinx, EDK, Code Composer Studio 3.0, Chip Scope Pro, gcc, Cross compiler Toolchain PowerPC405
Lead time	11 months